6.7 A 14-band Frequency Synthesizer for MB-OFDM UWB Application

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Multi-band orthogonal frequency-division multiplexing (MB-OFDM) UWB systems partition the 3.1 to 10.6GHz band into 14 sub-bands of 528MHz width [1]. Based on the system requirements [1], the UWB synthesizer demands a fast switching speed (<9.5ns). Several frequency synthesizers have been presented for 3 to 8GHz bands [2-5]. However, none can cover all 14 sub-bands. In this paper, a multi-band frequency synthesizer that uses two phase-locked loops (PLLs) is presented. This synthesizer generates all 14 carriers with sufficient sideband rejection and its frequency switching time is less than 3ns.

The proposed frequency synthesizer is composed of two PLLs, three single-sideband (SSB) mixers and two multiplexers as shown in Fig. 6.7.1. The full spectrum is partitioned into five groups and every group except for the fifth one has 3 sub-bands. The 3 sub-bands in the first group are realized by the first PLL (PLL1) and the first mixer (Mixer1). PLL1 generates the center frequency of 3960MHz in the first group and the second PLL (PLL2) realizes the band spacing frequency of 528MHz and the group spacing frequencies of 6336MHz, 3168MHz, and 1584MHz. Then, the second, third and fifth groups are obtained from the second mixer (Mixer2) by up-converting the first group with the group spacing frequencies. The fourth group is obtained from the third mixer (mixer3) by down-converting the fifth group with the group spacing frequency of 1584MHz. This frequency generation scheme makes the first-order unwanted sidebands caused by mixing fall outside the 7.5GHz spectrum so that a lower spur level is achieved.

To generate all the required quadrature signals for the SSB mixers, 4-stage ring oscillators are adopted in these two PLLs. In fact, these two PLLs only need to operate at 1980MHz and 3168MHz, respectively, which are half of the frequencies needed. The second harmonics are obtained from the drains of the tail current sources in the NMOS differential buffers. Using harmonics saves chip area and power consumption.

In PLL2, the band spacing frequency of 528MHz must be generated from a divide-by-3 circuit. Traditional static divide-by-3 circuits introduce tremendous distortion and may not be suitable for SSB mixers. There is also a regenerative divider for UWB applications [3], however the spurious performance is poor. To solve this problem, a quadrature divide-by-3 circuit is used and its single-ended version is illustrated in Fig. 6.7.2. It is composed of two 3-stage oscillators. The latch is adopted from [6]. The quadrature signals of 1584MHz are injected into this divide-by-3 circuit, and the output quadrature signals of 528MHz are obtained. To make sure that the phases of the output signals are in the desired order, phase-aligning buffers are inserted to avoid phase ambiguity. Such a divider generates precise quadrature signals with equal amplitude. By using this divider and a SSB mixer with switched-capacitor *LC* tanks, a sideband rejection over 40dB is achieved for every group.

The bandwidth requirement for both mixer1 and mixer3 is 1584MHz and they are realized by a conventional SSB mixer with switched-capacitor *LC* tanks [5]. However, mixer2 has to have a wide bandwidth of 6GHz and it should provide sufficient selectivity to lower the sideband level. Traditional shunt- and series-peaking techniques provide a wide and flat response, but lack enough voltage gain and selectivity. Single switched-capacitor *LC* tank mixers suffer from gain and selectivity degradation due to the decreased quality factor at lower frequencies. To alleviate this problem, mixer2 is realized by a 2-stage SSB mixer as shown in Fig. 6.7.3. Two switched-capacitor *LC* tanks can be programmed to the desired group and still have flat enough voltage gain. The gain varies by less than 3dB in every group. This circuit also provides a –80dB roll-off on the undesired group so as to provide better sideband rejection than a single *LC* tank.

This frequency synthesizer has been fabricated in 0.18μm CMOS technology. The die micrograph is shown in Fig. 6.7.4. The core area is 1.2×1.27mm^2. Symmetric inductors are utilized to minimize die area. The unwanted sideband level caused by frequency mixing is minimized by symmetric layouts. This chip is mounted directly on a PCB and draws 90mA from a 1.8V power supply.

There are 2 types of spurs in this synthesizer. One type of spur is caused by the frequency mixing with 528MHz in mixer1. Hence, the spurs in the first group will decide those in other groups. Figure 6.7.5 shows the sideband rejection at 4488MHz. Mixer1 provides 40dB suppression of the unwanted sidebands. The other type of spur is due to cascading mixers. Although first-order unwanted sidebands have been prevented by the frequency generation scheme in Fig. 6.7.1, higher-order spurious tones must be taken into consideration when the groups are up-converted by mixer2 and mixer3. The worst case occurs in the third group. The 3rd harmonics on the RF and LO ports of mixer2 will generate spurs in the adjacent group. The frequencies of the spurious tones are given as

$$f_1 = 3 \cdot f_{RF} - f_{LO} \text{ and } \quad f_2 = 3 \cdot f_{LO} - f_{RF} .$$

With the center frequency of 7128MHz in the third group, the RF frequency is 3960MHz and the LO frequency is 3168MHz, which introduces spurs at 8712 and 5544MHz. In Fig. 6.7.6, this effect can be observed by monitoring the whole UWB spectrum and noting that the sideband rejection is over 35 dB because the 2-stage SSB mixer was used. The band switching behavior is shown in Fig. 6.7.7 and the frequency switching time is below 3ns.

Acknowledgements:
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[3] C.C. Lin and C.K. Wang, "A Regenerative Semi-Dynamic Frequency Divider for Mode-1 MB-OFDM UWB Hopping Carrier Generation," *ISSCC Dig. Tech. Papers*, pp. 206-207, Feb., 2005.
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[6] R. Magoon and A. Molnar, "RF Local Oscillator Path for GSM Direct Conversion Transceiver with True 50% Duty Ccycle Divide by Three and Active Third Harmonic Cancellation," *IEEE RFIC Symp.*, pp. 23-26, June, 2002

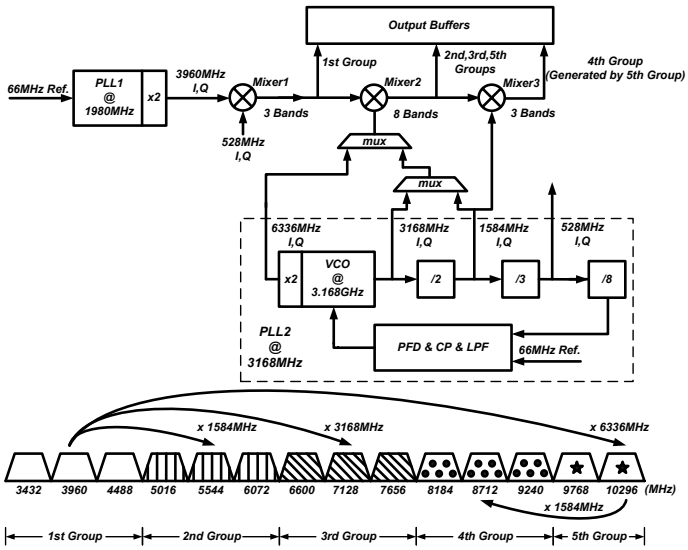

Figure 6.7.1: The synthesizer and its frequency plan.

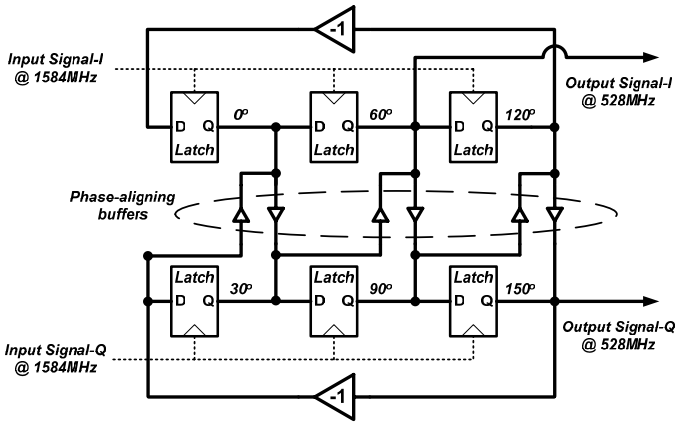

Figure 6.7.2: Single-ended version of the quadrature divide-by-3 circuit.

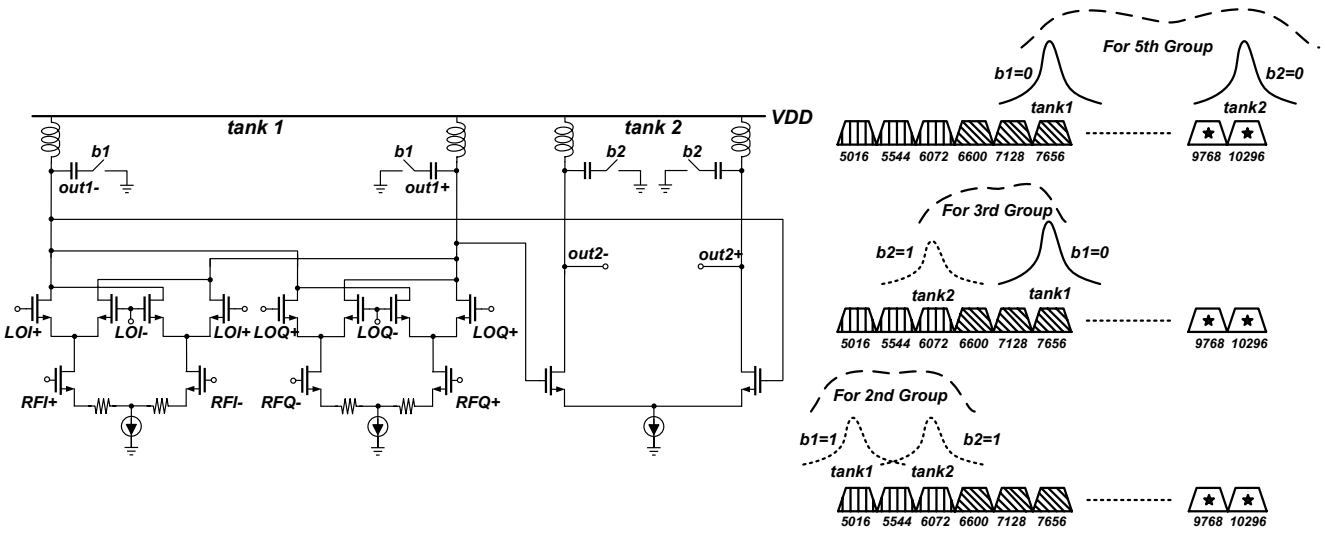

Figure 6.7.3: The second mixer and its operating principle.

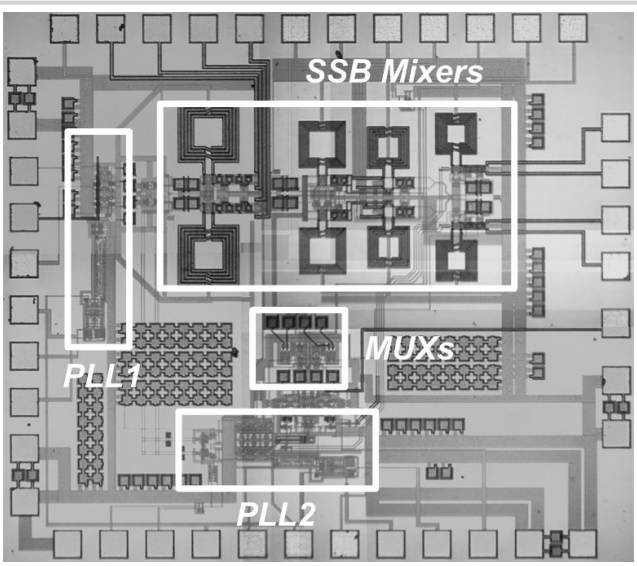

Figure 6.7.4: Die micrograph.

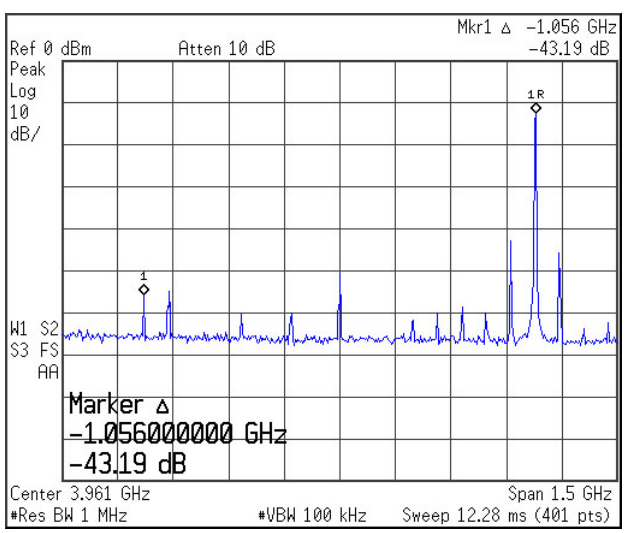

Figure 6.7.5: Measured SSB mixer1's spurs in the first group (<-40dB).

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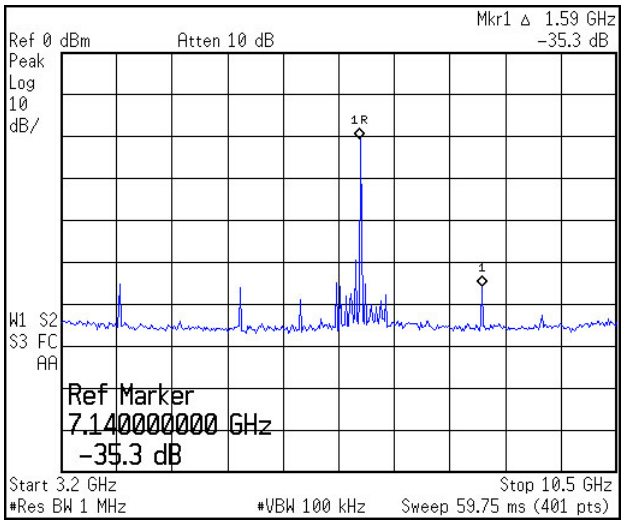

Figure 6.7.6: Spurs due to group mixing (full UWB spectrum).

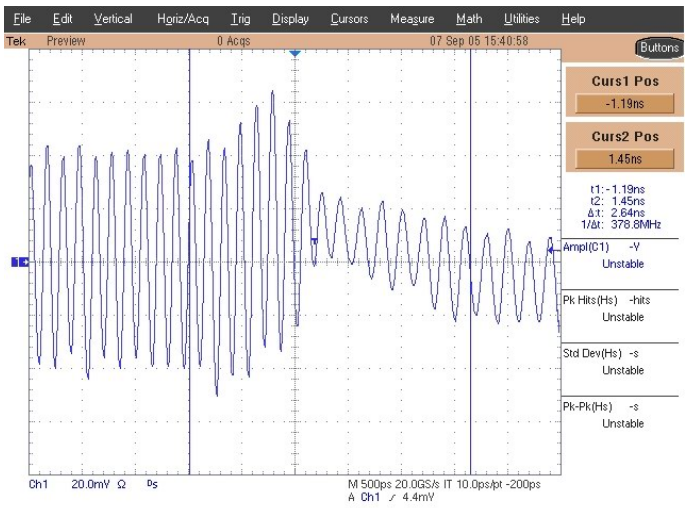

Figure 6.7.7: Frequency switching behavior (<3ns).

